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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,481	03/23/2005	Joo-Sun Yoon	AB-1379 US	1790

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MACPHERSON KWOK CHEN & HEID LLP
1762 TECHNOLOGY DRIVE, SUITE 226
SAN JOSE, CA 95110

EXAMINER	
ULLAH, ELIAS	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 12/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/509,481	YOON ET AL.	
	Examiner	Art Unit	
	Elias Ullah	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *East search history*.

DETAILED ACTION
Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, 5-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (6,188,452).

With respect to claim 1, Kim et al. teaches claimed a method of manufacturing a thin film transistor array panel for a liquid crystal display, the method comprising a forming a gate wire including a gate line and gate electrode connected to the gate line, depositing gate insulating layer, forming a semiconductor layer (Abstract, lines 1-10; Fig. 16H), forming a data wire including a data line intersecting the gate line to define a pixel area (Col. 5, lines 55-60), a source electrode connected to the data line and placed close to the gate electrode, drain electrode place opposite the source electrode with respect to the gate electrodes (claim 1), depositing a protective layer covering the gate wire or the data wire; forming an organic insulating layer by spin-coating an organic insulating material on the protective layer (Col. 4, lines 45-55); patterning the organic insulating layer for a first contact hole exposing the protective layer opposite the drain electrode (Fig. 15a, 15b); surface-treating the organic insulating layer by plasma

process using inactive gas (Claims 1-2); patterning the protective layer to form a second contact hole exposing the drain electrode and located inside the first contact hole; and forming a pixel electrode electrically connected to the drain electrode through the first and second contact holes (Col. 3, lines 10-25).

With respect to Claim 5, Kim et al. further teaches that the semiconductor layer comprises amorphous silicon or polysilicon (Fig. 17a; Col. 1, lines 50-60).

With respect to claim 6, Kim et al further teaches that the gate wire further includes a gate pad connected to one end of the gate line, the data wire further includes a data pad connected to one end of the data line, and the protective layer or the gate insulating layer has a third contact hole exposing the gate pad or the data pad, and wherein the thin film transistor array panel further comprise a subsidiary pad electrically connected to the gate pad or the data pad through the third contact hole and including substantially the same layer as the pixel electrode (Col. 3, lines 1-25).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (6,188,452) in view of Kobayashi et al. (5,767,827).

With respect to Claim 2-4, Kim et al. teaches the invention set forth above and further teaches amorphous silicon (Fig. 17a). But Kim et al. fails to disclose the

transparent conductive electrode or a reflective conductive film. Kobayashi teaches that the pixel electrode comprises a transparent conductive electrode or a reflective conductive film, a surface of the organic insulating layer has an unevenness pattern when the pixel electrode has the reflective film, and that reflective film has an aperture in the pixel area when the pixel electrode comprises both the transparent electrode and the reflective film (Col. 1, lines 40-65). In view of this disclosure, it would be obvious to one of ordinary skill in the art at the time the invention was made to have an aperture in the pixel area when the pixel electrode comprises both the transparent electrode and the reflective film because in such a way pixel electrode can be made from transparent electrode and the reflective film.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et all (6,188,452) in view of Park et al (6,184,070).

Kim et al. is applied as above but fails to expressly disclose wherein both the data wire and the semiconductor layer are formed by a photo etch seep using a photoresist pattern with position-dependent thickness.

Park et al. discloses a photo etch step using a photoresist pattern with position-dependent thickness (Col 2, lines 35-45). In view of this discloses, it would be obvious to one of ordinary skill in the art at the time the invention was made to use on etch step a photoresit pattern with position-dependent thickness because in such a way photoresist can be coated on the semiconductor layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Ullah whose telephone number is 571-272-1415. The examiner can normally be reached on 8-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MICHAEL LEBENTRITT can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Elias Ullah
Art Unit 2812

EMU

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER